

# EL

## Model EL8358MS 640 X 200 Pixel Electroluminescent Display

Operations Manual

### Product Profile

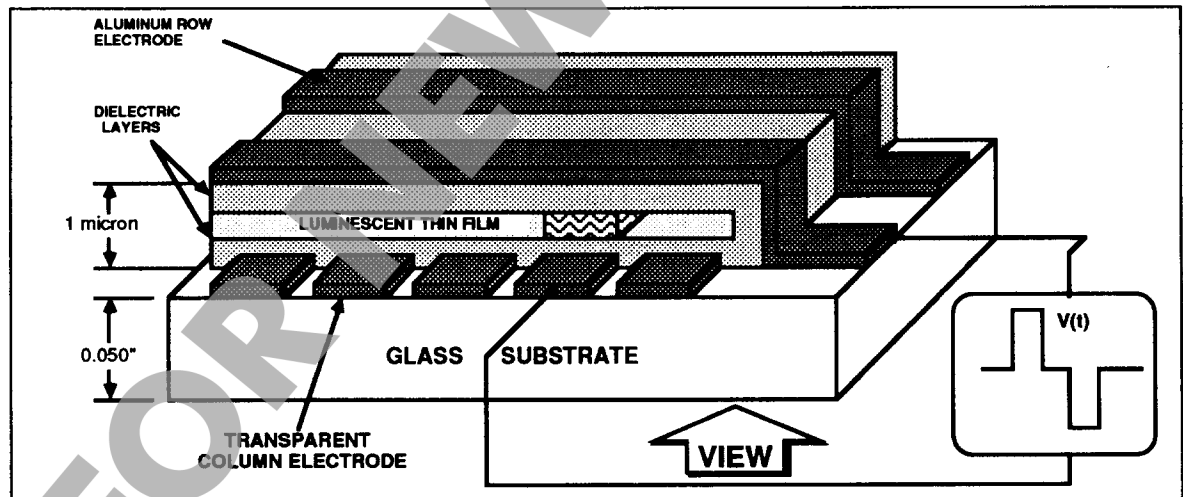
The EL8358MS is a compact, rugged, high-resolution electroluminescent (EL) display which replaces the bulky CRT for virtually all microcomputer-based product designs. Its compact dimensions keep overall system size to an economical minimum. It is designed to function in extreme environments, and its crisp display is viewable under most lighting conditions at wide viewing angles. It is easy to install and reduces system integration costs.

The EL8358MS is a 640 column by 200 row flat panel display. The pixel aspect ratio is 2:1, achieving complete compatibility with IBM CGA graphics software. The TTL-compatible interface is designed to match the needs of most digital or microprocessor-controlled systems.

The EL8358MS display requires DC power and four basic signals to operate:

1. Video Data or pixel information (VID),
2. Video Clock, pixel clock, or dot clock (VCLK),
3. Horizontal Sync (HSYNC) and
4. Vertical Sync (VSYNC).

### Technology



The display consists of an electroluminescent glass panel and a mounted circuit board with control electronics.

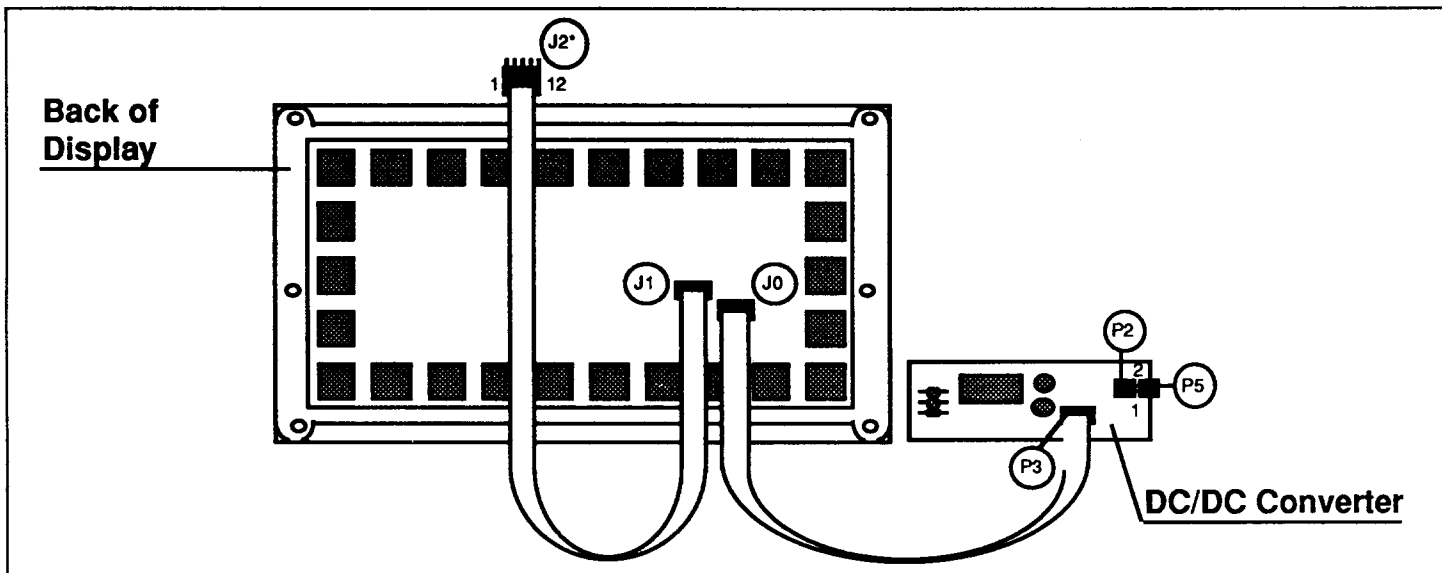
The EL glass panel is a solid-state device with a thin film luminescent layer sandwiched between transparent dielectric layers and a matrix of row and column electrodes. The row electrodes, in back, are aluminum; the column electrodes, in front, are transparent. The entire thin film device is deposited on a single glass substrate. A circuit board is connected to the back of the glass substrate. Components are mounted on this circuit board within the same area as the electroluminescent viewing area on the glass panel. The circuit board is connected to the glass with metal-on-elastomer interconnect technology. The result is a flat, compact, reliable and rugged display device.

In the EL8358MS, the 640 column electrodes and 200 row electrodes are arranged in an X-Y formation with the intersecting areas performing as pixels. Voltage must be applied to both the correct row electrode and the correct column electrode to cause a lit pixel. Operating voltages required are provided by a DC/DC converter.

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# Electrical Characteristics

The EL8358MS consists of a display, a universal DC/DC converter, and interconnecting cables as shown below.



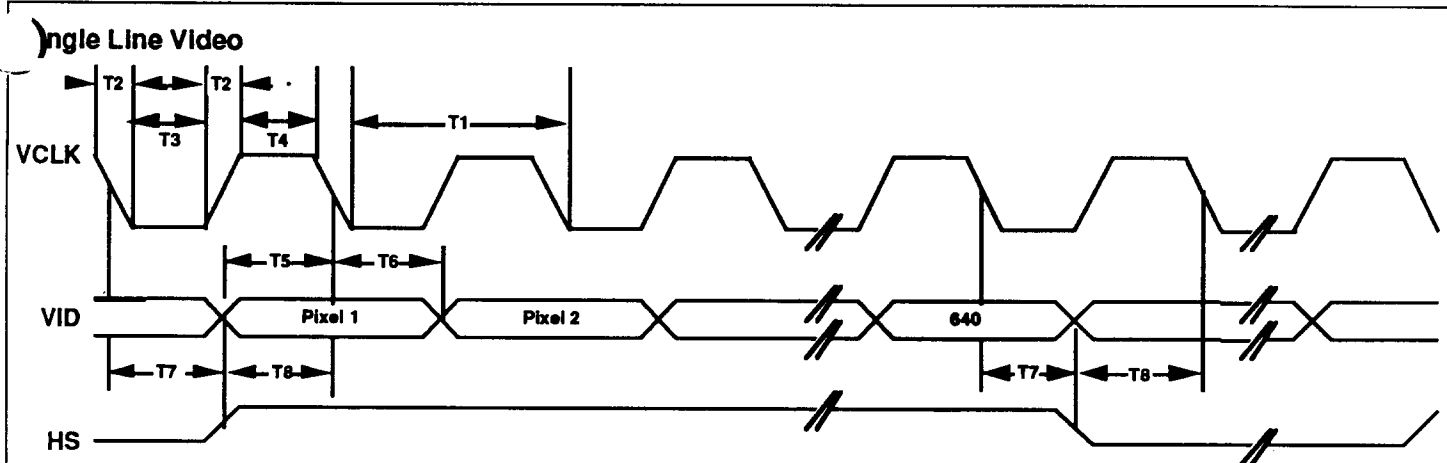
\* Note: Pins are reversed at J2 due to single-sided flat cable used.

## Display

### Video Input to Display at J1

Pin	Signal	Symbol	Description
1	Vertical Sync	VSYNC	A new frame is initiated by the rising edge of VSYNC. To properly sync the EL display, this edge must occur during the first horizontal sync high period of valid data for that frame.
2	Horizontal Sync	HSYNC	The rising edge of HSYNC marks the beginning of valid data for any given row while the falling edge marks the end of valid data for that row. HSYNC must be high during active (valid) video data. If HSYNC is high for more than 640 pixel clock periods, then the last 640 pixels prior to the fall of HSYNC will be visible on the EL display. HSYNC must contain an even number of VCLK periods.
3	Ground	GND	Signal return.
4	Video Data 2	VID2	VID 2 is only used when the optional two data line mode is selected; at that time, it contains the even pixel video data for the EL display. To use two data lines, DATASEL (pin 12) must be pulled to a TTL high (See VID1).
5	Ground	GND	Signal return.
6	Video Data	VID, VID1	Normally, with DATASEL low, VID contains the serial video data to be displayed on the EL display. When DATASEL is high (dual line mode) VID1 contains only odd-numbered pixel data. Pixel information on VID is supplied from left to right and from top to bottom; the first bit of data on VID at the beginning of a frame is displayed as the pixel at the upper left corner of the display. Bit number 640 is at the upper right corner. Bit number 641 is directly beneath pixel number 1 and so on.
7	Ground	GND	Signal return.
8	Video Clock	VCLK	VCLK provides the necessary signal to latch in the information present on VID. All control signals are referenced to VCLK.
9	Ground	GND	Signal return.
10	Video Clock Polarity	VCLKPOL	Sets the polarity of VCLK. When at a logic high, the pixel information must be valid on the falling edge of VCLK. When at a logic low, the pixel information must be valid on the rising edge of VCLK. If left open-circuit, it will automatically pull high into falling edge mode.
11	Video Polarity	VIDPOL	Selects the polarity of the video. When VIDPOL is high, the video is non-inverted. In this situation, a logic high (1) applied to a video input will result in a corresponding lit pixel on the EL display. When VIDPOL is low, the video is inverted, such that a logic low (0) applied to a video input will result in a corresponding lit pixel on the EL display. If left open-circuit, it will automatically pull high, into non-inverting mode.
12	Data Line Selection	DATASEL	Selects single line (logic low) or dual line (logic high) video mode. Dual line video mode allows pixel information to be presented to the display in a two-bit-wide parallel format with the VCLK at one half the single line video rate. If left open-circuit, it will automatically pull low into single line video mode.

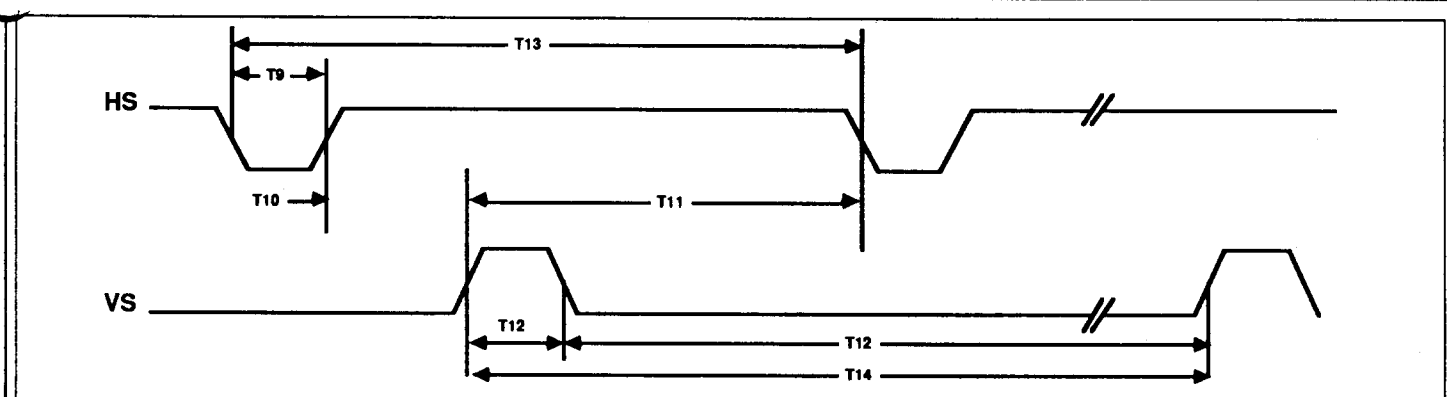
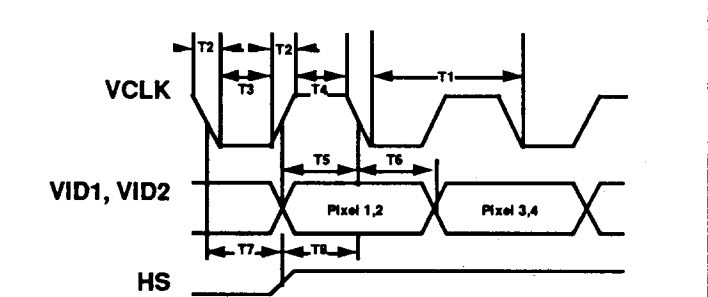
### Video Timing Input at J1



### Data Signals

Description		Single line: Dual line:		Units	
		Min	Max		Min
DATASEL control line		"0"	"1"		
T1	Video Clock period (tVCLK)	66	—	170	nsec
T2	VCLK rise, fall time (tRF)	—	10	—	10
T3	VCLK low width (tWL)	20	—	80	nsec
T4	VCLK high width (tWH)	20	—	90	nsec
T5	VID setup to VCLK (tSVID)	20	—	25	nsec
T6	VID hold from VCLK (tHVID)	20	—	105	nsec

### Dual Line Video



### Sync Signals

Independent of single/dual line mode:				
		Min	Max	Units
T7	HSYNC hold from VCLK (tHHS)	20	—	nsec
T8	HSYNC setup to VCLK fall (tSHS)	20	—	nsec
T9	HSYNC low time (VCLK must be running) (tHSL)	8	—	tVCLK
T10	VSYNC hold from HSYNC (tHVS)	0	—	nsec
T11	VSYNC setup to HSYNC (tVHS)	60	—	nsec
T12	VSYNC high/low width (tVsw)	1	—	tVCLK
T13	HSYNC period (tHS)	62	—	usec
T14	VSYNC period (tVS)	208	—	tHS
Frame Rate		—	77.5	Hz
(Typical vertical frame rate: 60Hz)				

### Video Electrical Specifications (TTL compatible)

Name	Parameter	Min.	Max	Units
Vil	input low voltage	-0.3	0.8	V
Vih	input high voltage	2.4	5.0	V
Iil	input low current	—	-0.4	mA
Iih	input high current	—	10	uA
Absolute Maximum		+5.5V		
Ta = 0°C to 55°C unless otherwise stated				

**Note:** All inputs except VIDPOL, VCLKPOL and DATASEL are TTL-compatible CMOS with 24KΩ pull-up resistors and 100Ω series resistors (to minimize under- and over-shoot of input signals). VIDPOL and VCLKPOL have TTL-compatible voltage levels with 2.4KΩ pull-ups. DATASEL has TTL-compatible voltage levels with a 1KΩ pull-down to ground.

## DC/DC Converter

The display and DC/DC converter are matched at the factory. Replacements to these matched units must be adjusted according to specifications. Consult Planar for design specifications.

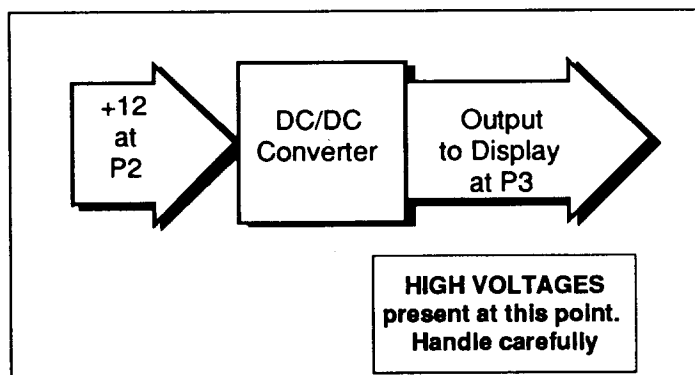
### Power Input to DC/DC Converter at P2

Pin	Signal/Symbol	Description
1	VH	Power supply input.
2	GND	Power return

### DC Power Input Specifications

Description	Min	Nom	Max	Units
Input voltage (VH)	11.4	12.0	12.6	VDC
Input voltage absolute max. (VH)	-	-	15.0	VDC
Input current (IH) (Vh=Min)	-	-	1.8	A

Ta = 0°C to 55°C unless otherwise stated



### DC/DC Converter Calibration - PS12DSS

The DC/DC converter cannot be tested separately. It requires an active low enable signal from the display to activate the high voltage section. The display provides this signal after detecting the presence of video signals at its input.

Note: The +12V input is protected by a 125V 4A fast blow fuse, BEL MQ4 or equivalent.

The DC/DC converter has been properly calibrated at the factory to the EL display by means of a voltage output adjustment. The converter should not need adjustment in the field. If the DC/DC converter and display become separated the following procedure can be used to reset the proper voltage setting:

1. Ensure power to the DC/DC converter is off.
2. Turn the trimpot on the DC/DC converter fully counterclockwise (ccw).
3. Connect the DC/DC converter to the display using the 14 pin flat cable.

4. Apply a full on video pattern to the display (full white field). At the factory, calibration is done with all pixels on.

5. Set the DVM to measure a 235 VDC voltage.

6. Connect the positive DVM lead to V(ALL ON), pin 1 on P0. Be very careful not to short from pin 1 to pin 2, as pin 2 is ground. Connect the ground lead of the DVM to a more convenient ground on P0 pin 12. See the drawing on page 7.

7. Apply power to the DC/DC converter.

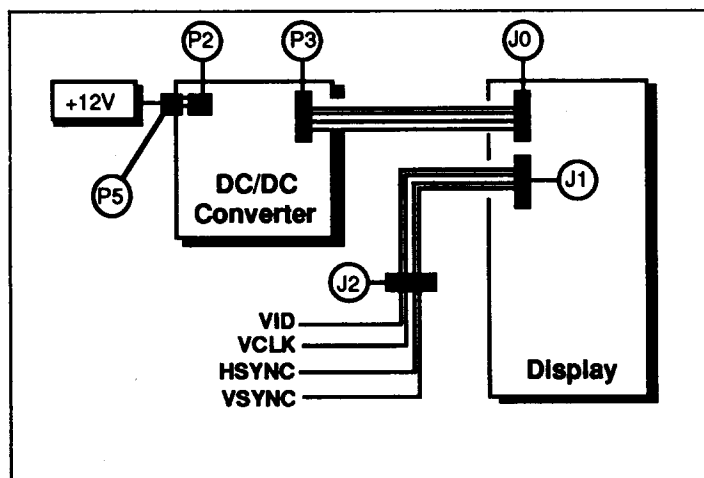
8. Note the voltage statement on the display. A sample is shown at right:

PS SN: \_\_\_\_\_  
V (ALL ON): + \_\_\_\_\_

9. Adjust the trimpot on the DC/DC converter clockwise (cw) until the voltage reading of the DVM is equal to the V (ALL ON) voltage  $\pm 1V$ , as specified on the display. Do not exceed 235V.

10. Calibration is complete.

## Interconnections



Connector	Manufacturer	Manufacturer's Model Number
J0	Burndy	SLEM14R-2 or equivalent
J1	Burndy	SLEM12R-2 or equivalent
J2	Burndy	SLEM12R-2 or equivalent
P2	Molex	22-11-2022 or equivalent
P3	Burndy	SLEM14S-2 or equivalent
P5	Molex	Housing: 22-01-3027 or equivalent (customer-supplied) Crimp Terminals: 08-55-0102 or equiv.
Cable	Manufacturer	Manufacturer's Model Number
J1-J2	Gore	BMS-829-1-12-X or equivalent
J0-P3	Gore	BMS-829-1-14-X or equivalent

# Operational Specifications

## Environmental

### Temperature

Operating	0°C to +55°C
Operating Survival	0°C to +70°C
Non-Operating	-55°C to +75°C

The EL display will function at operating survival temperatures for a 24-hour period and incur no damage but may not meet some specifications above the +55°C operating limit.

### Humidity

95% relative humidity (non-condensing) as verified by MIL-STD-202F method 106E.

### Altitude

Operating	25,000 ft. (7,620 m) above sea level
Non-Operating	100,000 ft. (30,480 m) above sea level
Non-Operating Pressure	6 Atm for 1 hour

### Vibration (Operating)

<b>5–25 Hz:</b>	
Sweeptime	10 min ea. axis, 1 min sweep rate
Amplitude	0.100 inches p-p displacement
Dwell at resonance	15 min each axis
If no resonance is found, dwell is performed at 55Hz, 0.0600 inches p-p displacement, for 15 minutes.	

<b>25–55 Hz :</b>	
Sweeptime	5 min ea. axis, 1 min sweep rate
Amplitude	0.060 inches p-p displacement
Dwell at resonance	15 min each axis
If no resonance is found, dwell is performed at 55Hz, 0.0600 inches p-p displacement, for 15 minutes.	

### Vibration (Non-operating)

<b>55–500 Hz:</b>	
Sweeptime	120 min ea. axis, 3.2 min sweep rate
Amplitude	3 g peak acceleration
Dwell at resonance	30 min each axis
Dwell is performed at all resonances of $g(\text{out})/g(\text{in}) \geq 5$ .	

### Shock

Magnitude	50 g peak acceleration
Duration	11 ms (half sine wave)
Number of tests	3 on each of 6 surfaces

### Mean Time to Failure

Greater than 30,000 hours

### Electromagnetic Compatibility

The display is capable of being operated in a final product that complies with FCC Docket, Part 15, Subpart J, class B.

## Optical

### Display Color

Peak emission wavelength	585nm (Yellow-Orange)
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### Pixel Luminance

ON luminance	Typical 38 fL (130 cd/m <sup>2</sup> pixel) Minimum 30 fL (103 cd/m <sup>2</sup> pixel)
Luminance measured at center of display screen, 60 Hz full ON pattern, 25°C ambient temperature.	

OFF luminance	0.3 fL maximum (1.0 cd/m <sup>2</sup> pixel)
Luminance measured at center of display screen, 60 Hz full OFF pattern, 25°C ambient temperature.	

ON luminance uniformity	Maximum difference $\leq 26\%$ Measured between any two of five points (corners and center): Non-uniformity % = $(1 - \text{min luminance}/\text{max luminance}) \times 100$ .
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ON luminance variation (temp.)	Maximum variation $\pm 15\%$ From 25°C over 0°C to +55°C range.
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ON luminance variation (time)	Maximum difference $\pm 10\%$ At 25°C within 10,000 hours.
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### Fill Factor

55.5% luminance area/total active area.

### Viewing Angle

Greater than 160° viewing cone (80° viewing angle for all axis about the normal display face).

### Optional Filter

For best overall performance in high or low light levels, an amber or neutral gray circular polarizing filter with anti-reflective coating or etch is the usual choice. This filter will make the reflective electrodes of the display darker and will improve the contrast ratio. The anti-reflective coating on the filter should face the user, and the tape side of the filter should face the display.

## Safety and Health

### Safety

The display will not inhibit the end product from obtaining any of the following certifications: UL114/478, CSA 154, IEC 380.

### Health

An inert, non-toxic, silicon-based oil is used in the construction of the electroluminescent panel.

## Installation and Handling

### Unpacking

#### Electrostatic Caution

The display and DC/DC converter assemblies use CMOS and power MOS-FET devices. These components are electrostatic sensitive. Unpack, assemble and examine these assemblies in a static-controlled area only. When shipping either assembly, use packing materials designed for protection of electrostatic-sensitive components.

Unpack and check contents of shipping container against invoice in a static-controlled area. Use anti-static bags for storage of displays and DC/DC converters awaiting assembly processes. Any discrepancies in materials received and invoiced should be noted to Planar Systems, Inc. within 10 days.

### Mounting and Connector Locations

As shown on Page 7, this unit has six mounting holes, three located on each side of the display. When mounting the display, use all six of these holes; failure to do so will invalidate the product warranty. To avoid breaking the glass, use appropriate length standoffs and avoid deflecting the mounting holes out of the plane of the display when tightening the mounting hardware. The vibration and shock specifications listed on Page 5 are accurate only if all six mounting holes are used.

Install the flat flex cables with the exposed conductors toward the wide side of the connector slot.

### Cleaning

Display Face	Any non-abrasive mild glass cleaner can be used.
Filter	Do not clean the Planar-supplied acrylic filter with alcohol.
Circuit Boards	Only isopropyl alcohol should be used on the ECB assemblies.

### Avoiding Burn-in

As with any other display, it is prudent to use screen-saver software to avoid burn-in of images that remain on the screen for extended periods.

## Mechanical Characteristics

### Display External Dimensions

Height	6.95 in.	176 mm
Width	10.53 in.	267 mm
Depth	0.67 in.	17 mm
Weight	24 oz. max	680 grams

Recommended air gap behind monitor places total depth at 1.0".

### DC/DC Converter Characteristics

Height	2.00 in.	51 mm
Width	5.70 in.	145 mm
Depth	1.25 in.	32 mm
Weight	5 oz. max	140 grams

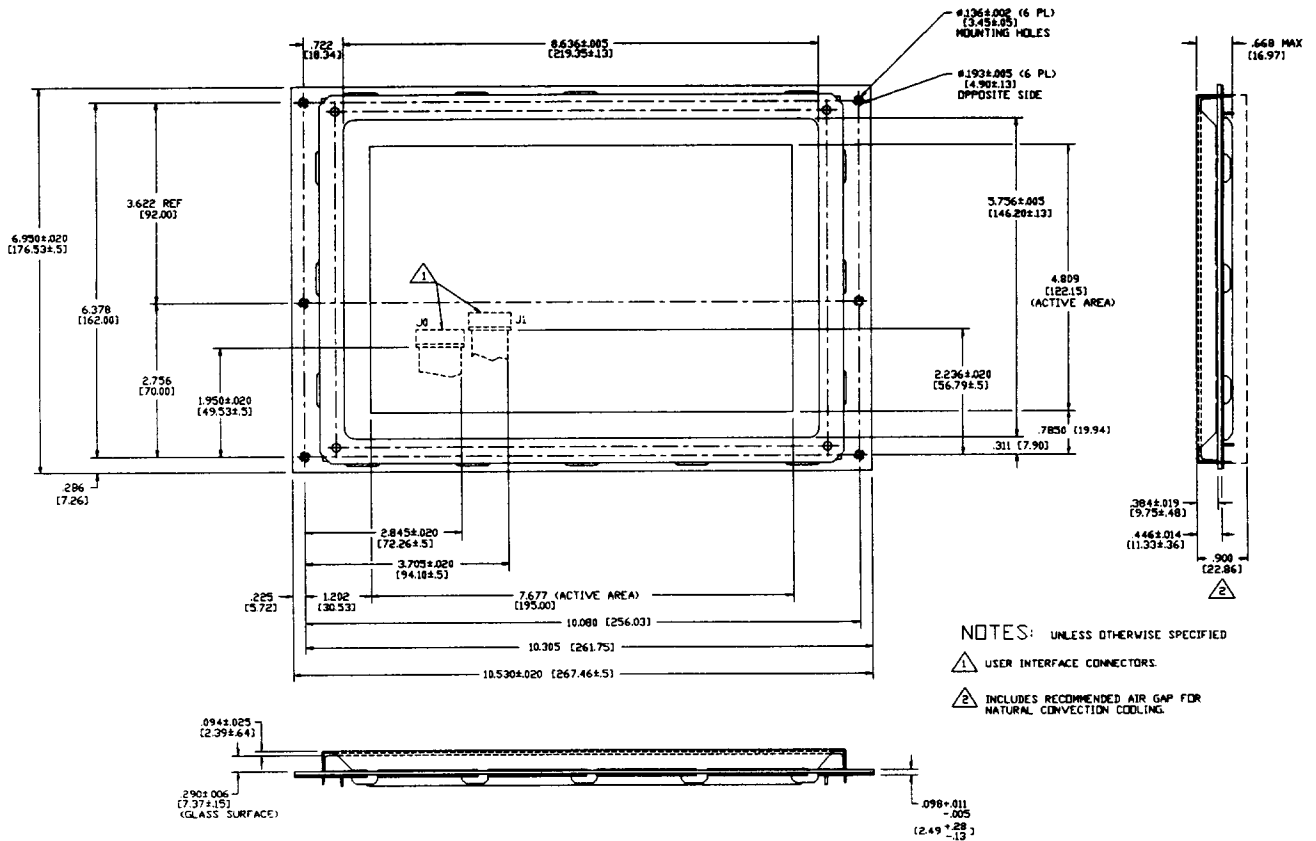
### Display Viewing Area Characteristics

Active Area	Height	4.796 in.	121.8 mm
	Width	7.676 in.	195.1 mm
Pixel pitch	Height	0.024 in.	0.610 mm
	Width	0.012 in.	0.305 mm
Pixel size	Height	0.020 in.	0.508 mm
	Width	0.008 in.	0.203 mm

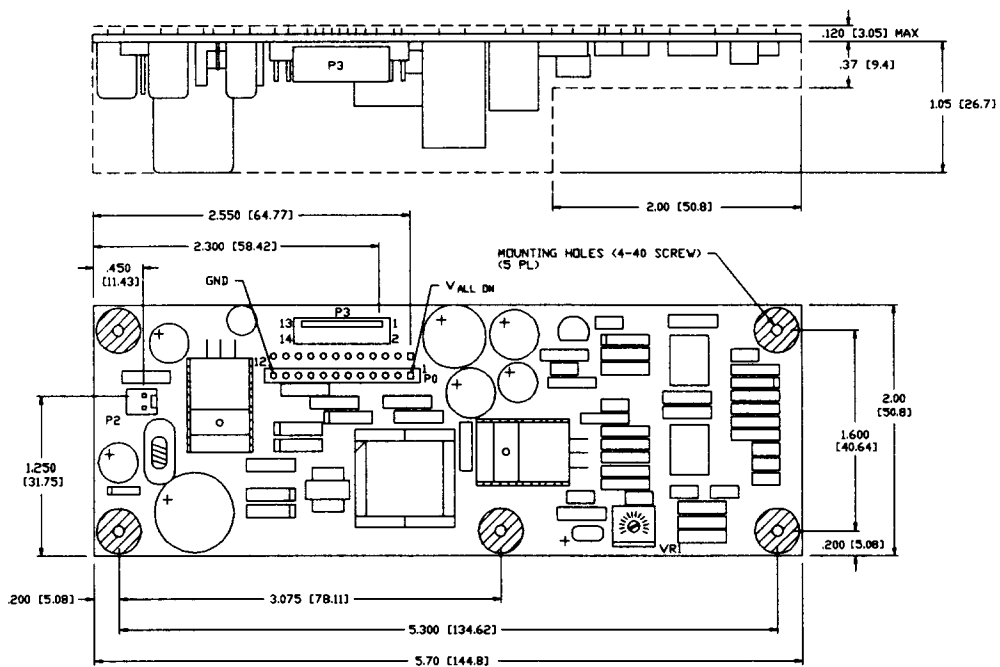
Pixel matrix organization:

640 pixels horizontal by 200 pixels vertical

### Display External Dimensions



### DC/DC Converter - PS12DSS



## Description of Warranty

This description is not the full warranty, and should not be construed as a substitute for the full warranty. A copy of the full warranty is available upon request.

Planar warrants that the goods it sells will be free of defects in materials and workmanship, and that these goods will substantially conform to the specifications furnished by Planar, and to any drawings or specifications furnished to the Seller by the Buyer if approved by the Seller. This warranty is effective only if Planar receives notice of such defect or nonconformance during the period of warranty, which begins the day of delivery.

The goods Planar sells are warranted for a period of one year unless otherwise agreed to by Planar and the Buyer. The Buyer must return the defective or nonconforming goods, upon request, to Planar not later than 30 days after Planar's receipt of notice of the alleged defect or noncompliance. Buyer shall prepay transportation charges, and Planar shall pay for return of the goods to the Buyer. No goods are to be returned to Planar without prior written permission.

The warranty does not apply in cases of improper or inadequate maintenance by the Buyer, unauthorized modification of the goods, operation of the goods outside their environmental specifications, neglect or abuse of the goods, or modification or integration with other goods not covered by a Planar warranty when such modification or integration increases the likelihood of damage of the goods.

Represented by:

North American sales contact:

### **Planar Systems, Inc.**

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European and Far East sales contact:

### **Planar International Ltd.**

Olarinluoma 9  
P.O. Box 46  
SF-02201 Espoo, Finland  
Phone: 358 0 420 01  
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## Easy to Use

There are many options available which make Planar EL displays easy to use, easy to interface, and easy to package. Examples of options which are typically available include RS232 Interface Adapter, IBM XT/AT Interface Adapter, IBM PS/2 Interface Adapter, Touch Bezels, Metallic Enclosures and AC Power Supplies. Call Planar for complete information and availability.

## Support and Service

Planar Systems, Inc. is a U.S. company based in Beaverton, Oregon and Espoo, Finland with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Planar displays as simple and quick as possible for our customers.

**RMA Procedure:** For a Returned Material Authorization number, please contact Planar Customer Service Department, with the model number(s) and original purchase order number(s). When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

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